Heavy Ion SEE Tests for Texas Instruments ADS5483 ADC

Principal Investigator: Melanie Berg, MEI Technologies
Test Engineers: Melanie Berg, Hak Kim, and Anthony Phan MEI Technologies

Initial Plan Submitted:
Plan Updated:
Test Set-up Demo Date:
Test Date:

I. Introduction

This study is being undertaken to determine the Single Event Effects (SEE), susceptibility of the Texas Instrument ADC converter: ADS5483. The Devices Under Test (DUTs) will be evaluated with heavy ions and protons.

II. Devices Tested

There was a total of xxxxxx ADC tested. 2 were made available for heavy ion testing, including 1 control sample. 4 devices were made available for proton testing. Due to time constraints, we were not able to build a specialized DUT board. We used a Texas Instrument Evaluation board with one embedded ADC (DUT). The Evaluation board number is ADS548xEVM. The identification information for these ADCs is as follows:

Test Chip: ADS5483

Lot # xx

The device technology is Texas Instruments complementary bipolar process BiCom3x. The following are some of the ADS5483 Features (please refer to the ADS5483 datasheet for a complete description):

- 16-bit resolution. 78 dBFS Noise Floor
- 170MSPS Sample Rate
- SFDR = 95dBc
- On-Chip High Impedance Analog Buffer
- Efficient DDR LVDS-Compatible Outputs
- Power-Down Mode: 70mW
- Industrial Temperature Range: -40C to 85C
- 3 Vpp Differential Input Range
- 5v or 3.3 V Power supply

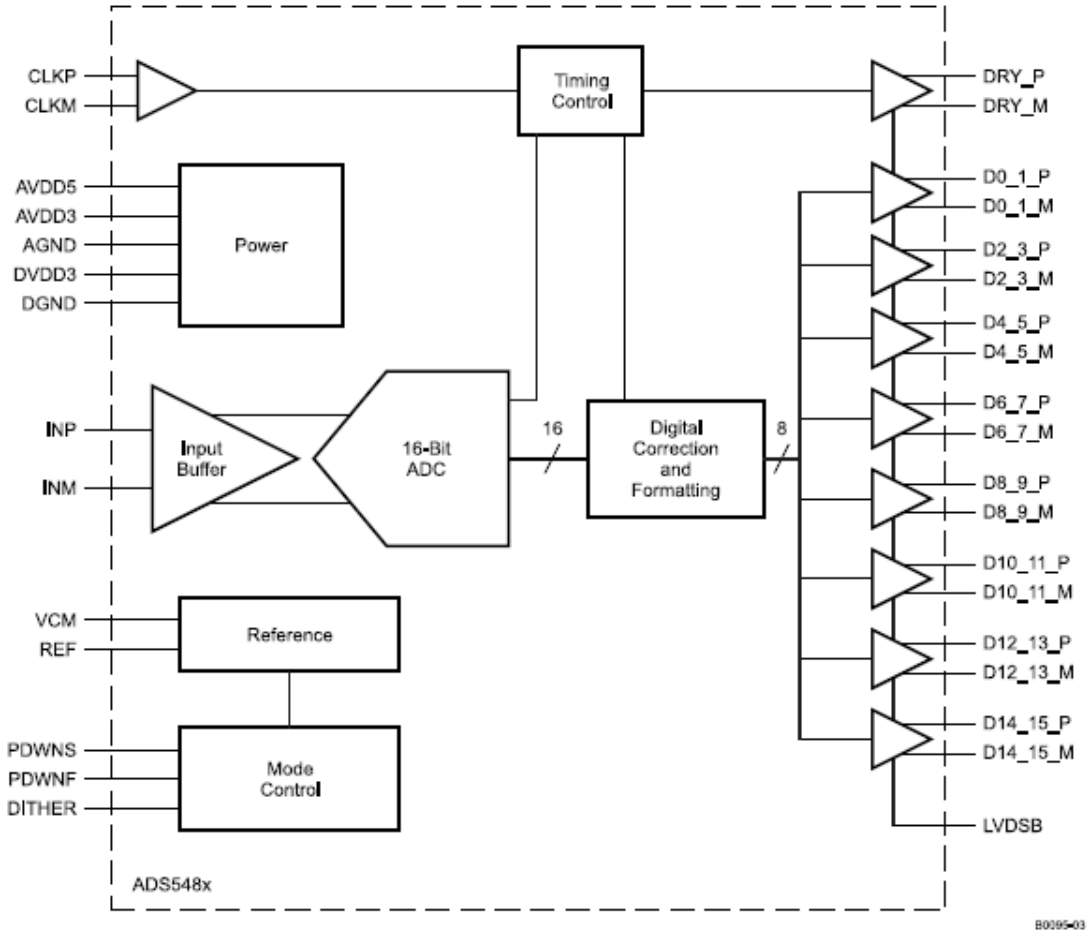
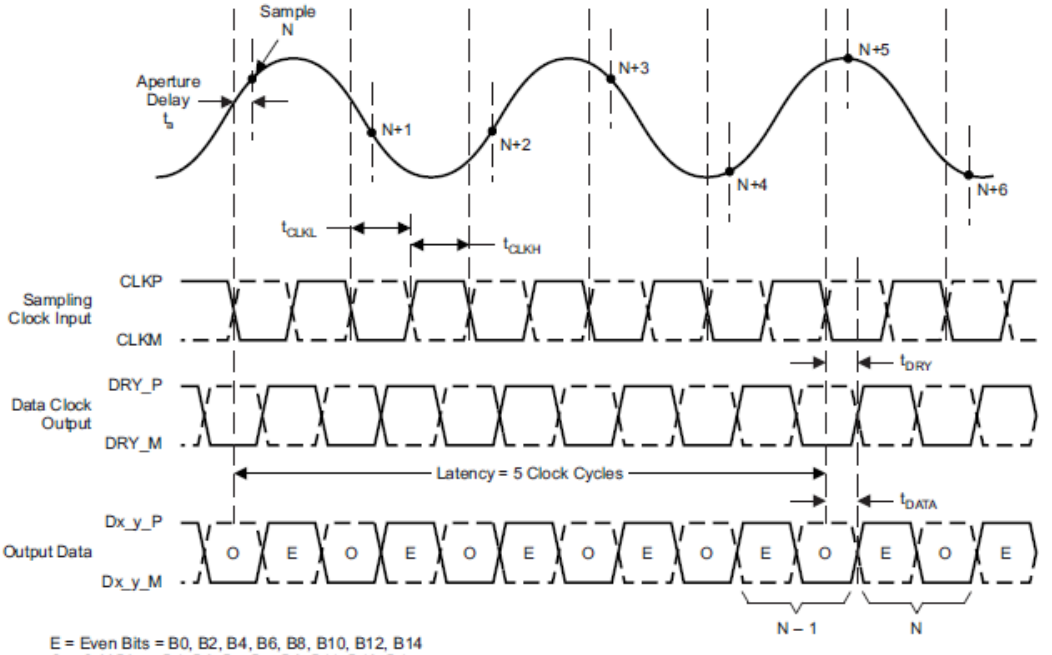


Figure 1: Functional Block Diagram of the ADS5483

TIMING INFORMATION



E = Even Bits = B0, B2, B4, B6, B8, B10, B12, B14
O = Odd Bits = B1, B3, B5, B7, B9, B11, B13, B15
Dx_y_P/M are LVDS outputs that have two bits per pair (EVEN and ODD). The values for x and y are 0_1, 2_3, 4_5, ... 14_15.

TD158-02

Figure 1. Timing Diagram

TIMING CHARACTERISTICS(1)

Typical values at T_A = 25°C: minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = max rated, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay			200		ps
	Aperture jitter, rms	Internal jitter of the ADC		80		fs
	Latency			5		cycles
t_{CLK}	Clock period	CLK = max rated clock for that part number	1e9/CLK		100	ns
t_{CLKH}	Clock pulse duration, high		0.5e9/CLK		50	ns
t_{CLKL}	Clock pulse duration, low		0.5e9/CLK		50	ns
t_{DRY}	CLK to DRY delay time(2)	Zero crossing, 5-pF parasitic to GND	1500	1900	2300	ps
t_{DATA}	CLK to DATA delay time(2)		1400	1900	2400	ps
t_{SKEW}	DATA to DRY skew	$t_{DATA} - t_{DRY}$, 5-pF parasitic to GND	–500	0	500	ps
t_{RISE}	DRY/DATA rise time	5-pF parasitic to GND		500		ps
t_{FALL}	DRY/DATA fall time			500		ps

(1) Timing parameters are assured by design or characterization, but not production tested.
(2) DRY and DATA are updated on the rising edge of CLK input. The latency must be added to t_{DATA} to determine the overall propagation delay.

Figure 2: Illustration of ADS5483 DDR Output

III. Test Methodology and Evaluation

Regardless of the test methodology employed during SEE evaluation, it is important to filter the non-SEU noise generated from the test vehicle and the ADC device. Consequently, if each test consists of comparing the ADC output code to an expected value, then compensation must be made due to inherent system error during the comparison process.

As a solution, prior to testing, system noise was measured for each test type. A minimal error-bound (EB) windowing each expected value was calculated per test set-up such that

no ADC output code errors exist during operation and pre-irradiation. The EB code value can be translated to its corresponding voltage level (V_{EB}) as illustrated in (1).

$$V_{EB} = \frac{EB*Vpp}{2^{Nb}} \quad (1)$$

Regarding (1), Nb is the number of ADC output bits and V_{pp} is the peak-to-peak manufacturer supplied voltage range (3V pp for the ADS5483).

Potential SEEs that fall within the EB window will not be observable. Therefore, to obtain maximum observability, it is essential to minimize test vehicle noise. EB values will change based on the test set-up, Number of ADC output bits, and the ADC DUT. SEE tests are performed with the minimum calculated EB, however, post processing of radiation data entails calculating SEU cross sections at various EB values so that:

1. SEU ADC cross sections obtained from different test vehicles with different noise characteristics can be compared by analyzing cross sections with common V_{EB} values.
2. SEU ADC cross sections obtained from different ADCs with a different number of output bits can be compared by analyzing cross sections with common V_{EB} values.
3. The amplitude of ADC SEU code errors can be better analyzed. As an example, histograms can be developed binning amplitude errors within particular ranges.

The following sections will discuss two test methodologies that were implemented for ADS5483 SEE evaluation. As previously stated, all SEE tests utilized minimal EBs during radiation tests.

A. Single Point (SP) Test Scheme

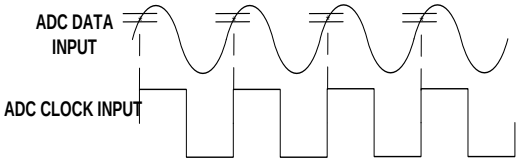


Fig. 3: Single Point - Clock and Data are the Same Frequency. Actual clock is the same sinusoid as the data input but is illustrated as a square wave for simplification of demonstrating sampling points.

The REAG approach to SP ADC SEE testing is to apply input excitation to the ADC clock and data connections from the same source (i.e. clock and data input signals are tied together). Clock frequency, f_s, is strictly equal to data frequency, f_d. Consequently, the ADC will theoretically always sample the same point as illustrated in Fig. 3. As a result, the data output of the ADC should stay near constant.

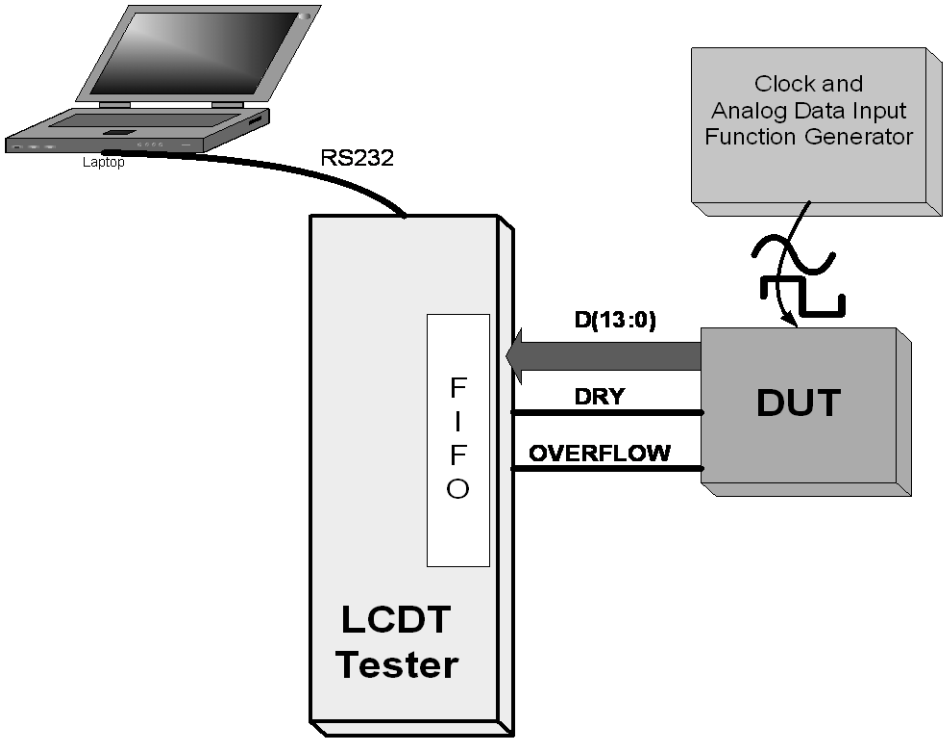


Figure 4: Tester to LCDT Topology

1. SP Implementation

Figure 4 illustrates the test set-up. There is a user pc to supply the commands (such as start test, reset, and other test parameters (i.e. frequency control). There is one frequency generator that supplies one sinusoid signal that is passed through a T connector to both the ADC clock and data input. No synchronizer is necessary because the clock and data are the same signal. The tester is used purely to gather output data response from the evaluation board. Data is collected at every edge of DRY (DDR outputs) see Figure 1. Each ADC output data item is compared to an expected value. If there is an error (mismatch), then the data item is time stamped and sent (with its associated expected value) to the user PC via the RS232 interface.

2. SP Expected Value Calculation

Before the DUT is irradiated for each test, approximately $1x10^6$ ADC output data points are read by the tester. Because the set-up is in SP mode, there is one expected value (E) calculated. Equation 2 illustrates how the expected value is calculated

$$E = \frac{\sum_{n=1}^{N} Xn}{N} \qquad (2)$$

N= total number of points for expected value calculation (approximately $1x10^6$)
Xn = current sample
E= Expected Value (average of all ADC output points).

3. Data Compare to Expected Value

After the expected value is calculated, the tester automatically enters compare mode. All outputs of the ADC are now compared to the pre-calculated expected value.

This test becomes advantageous because data and clock are generated from the same source; SP is simple to set up and has minimal test vehicle noise. For a 14-bit ADC, a minimal EB of 16 (1.95mv) was calculated for the implemented test vehicle. Let E be the expected value and X_n the ADC output code, then (3) is the SP comparison performed for every X_n in the LCDT.

$$\left(E - EB/2\right) \le X_n < \left(E + EB/2\right); \qquad (3)$$

4. Clock loss

The DRY is constantly monitored. If a DRY misses a clock cycle (or more), then it is registered and the Tester sends a message to the host signifying a clock loss with its corresponding time stamp.

B. The Pros and Cons of SP testing

The benefit of the SP schemes is that it is relatively easy to implement. The methodology proves to be sufficient at counting errors during irradiation. As a result, general SEE error cross-sections are valid using this technique and are currently used in critical missions for upper bound ADC error prediction.

Because SEEs last for a discrete amount of time and are not consistent noise spread amongst all ADC input periods (as is ADC parametric noise), more information per ADC input data period (than that provided via SP) must be provided while investigating SEEs. Subsequently, the sampling frequency must be significantly higher than the input data frequency. As an example, in SP mode, because only one point per data period is sampled, the difference between jitter, flattening, or small perturbations to the output signal composition is difficult to differentiate. In addition, the longevity of the error is another essential portion of SEE data analysis.

C. Four Point (FP) Test Scheme

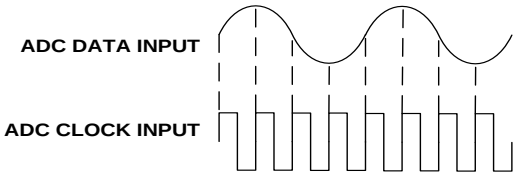


Fig. 5: Four Point ADC Clock and Data Waveforms. The actual clock is a sinusoid but is illustrated as a square wave for simplification of demonstrating sampling points.

As previously stated, evaluation of signal composition such as temporary signal flattening or temporary phase shifts requires more samples per data input period. As a simplified first approach, REAG developed the FP test scheme. The algorithm of the FP scheme dictates that the relationship of input clock (fs) to input data (fd) is $fs = 4 \cdot fd$ and is illustrated in Fig. 5. Consequently, four points are sampled per signal period.

As a direct result of over-sampling, the two dimensional nature of SEU errors (phase and amplitude) can be precisely tracked and critical design considerations can examined such as:

- Will the signal retain its composure (noisy output)?
- Is the phase of the output signal affected?
- Can there be complete loss of data output signal (flattening)?
- Will the signal filtration system require a more complex design implementation?

1. FP Implementation

The FP algorithm implemented within the FPGA tester core has two phases:
(1) Preprocessing that includes expected value calculations and
(2) Irradiation that includes filtration and data processing.

The FP technique requires constructing windows that are temporally 4 clock cycles long in order to simultaneously evaluate 4 consecutive ADC output samples. The samples are expected to track the input analog sine wave. The tester is able to evaluate every clock cycle of data and report every cycle of error. This facilitates burst analysis with the granularity of a clock cycle. A short list of the requirements pertaining to the FPGA of the test system:

- Expected values must be established (used as golden)
- Detection of clock loss must be added to tester
- Tester must be available to grab every cycle of ADC data
- Error data shall be sent to the host PC from the tester

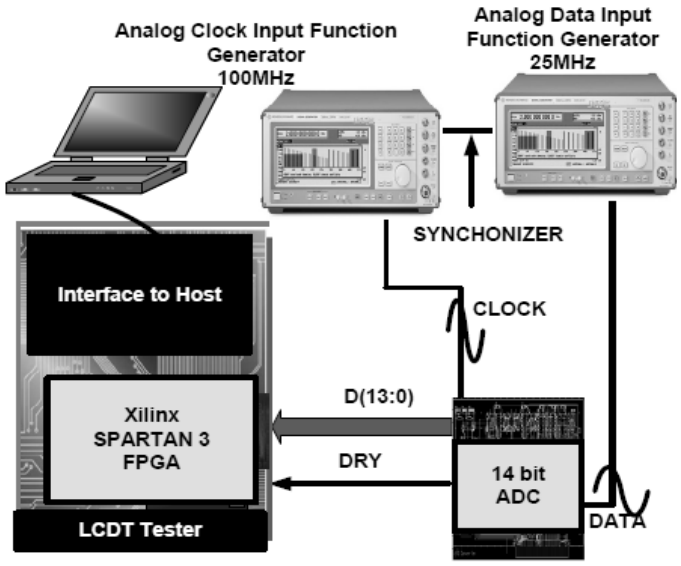


Fig. 6: LCDT Interface to DUT Schematic

2. Expected Value Calculations

A window is defined to cover one complete period of the input signal and is illustrated in Fig. 7. Because there are 4 sample points per window regarding the FP scheme, one window will have 4 bins (k=1,2,3,4) – one for each input sample. Each Sample is

accumulated into its designated bin (e.g. sample X_1 gets accumulated into bin k=1 and X_2 gets accumulated into bin k=2)

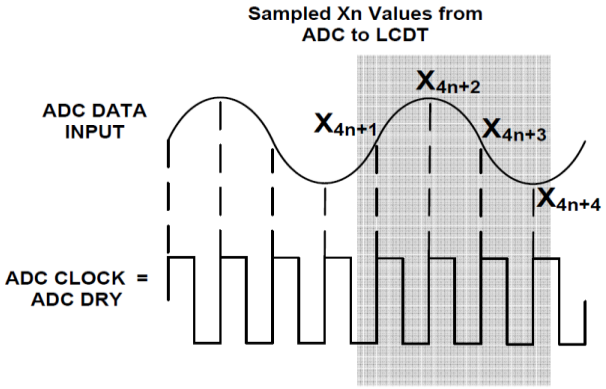


Fig. 7: Four Point ADC Clock and Data Waveforms

The average of each bin produces 4 expected values with E = (E_1, E_2, E_3, E_4) and is reflected in (4).

$$E_k = \frac{\sum_{n=0}^{Total-1} X_{4n+k}}{Total}; \quad k = (1,2,3,4) \tag{4}$$

The four expected points are calculated by the tester's FPGA after capturing 4,000,000 ADC output values (i.e. total = 1,000,000). The expected values are calculated at the beginning of each test and do not change during irradiation.

3. Data Compares to Expected Values during Irradiation

As the ADC output data is captured by the tester, it must be compared to expected values to determine if there is a fault at the DUT output. The comparison is performed as follows: For each window of four points, compare incoming sample points ($X_{m \bmod k}$) to expected values (E_k) (e.g. compare X_1 to E_1). The comparison formula performed by the LCDT is found in (5).

$$\left(E_k - EB\right) < X_{m \bmod k} < \left(E_k + EB\right); \quad k = (1,2,3,4); \quad m = (1,\infty) \tag{5}$$

Because data input is a sinusoid input, without SEE, there is a strict ordering of ADC outputs that is based off of point-to-point derivatives. Possible derivative orderings are listed in Fig. 8.

Fig. 8: Possible orderings of windowed 4-point Derivatives without error during Normal Operation

Regarding Fig. 8, the sign of the derivative is of importance not the actual value. The sign can be obtained by subtracting X_{n-1} from X_n.

4. Clock loss and Windowing

Because the ADC DRY output signal is a replica of the ADC input clock when data is available, clock loss is determined by monitoring the DRY ADC output signal. As

illustrated in Fig. 9, a clock loss can interrupt expected sequencing of incoming (to the tester) samples. This is a problem because a clock output can become inactive and become active at any point within the input signal period upon a SEE. Once data sequencing has been interrupted, the tester comparison circuitry can not assume that the first value of the window will be associated with the original X_1 data item. If nothing is done, then Therefore dynamic synchronization must be established so that

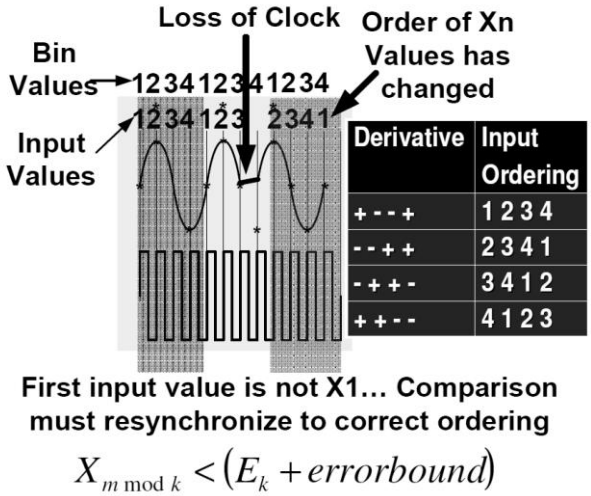


Fig. 9: FP Windows. Tester Synchronization Causes Order of Derivatives and Subsequent Expected Values to Change

5. Clock Loss and Data Synchronization…Dynamic Windowing

The previous section demonstrated how the order of ADC output values (tester input values) can change during a clock loss (e.g. E_1 no longer corresponds to X_1). In order to guarantee the correct sampled input is compared to the correct expected value, a novel approach had been developed called Dynamic Window Ordering (DWO). DWO is based off of the fact that because there are only 4 samples of a sinusoid input per window, there exist only 4 sample orders.

Each group of derivatives can directly be mapped into input ordering schemes. The premise is illustrated in Fig. 9. The figure shows how the input sequence starts with X_1 with its associated derivative sequence (e.g. +--+ →1 2 3 4). This implies that as the input values are captured, they should be compared to expected values E_1, E_2, E_3, E_4. The derivative sequence is calculated for each window (i.e. for every 4 input values). If a clock loss occurs, the window derivative sequence will change depending on how many lost clock cycles had occurred and will be kept track of by the tester. The example in Fig. 9 shows one clock cycle loss that results in the following window having an input sequence of X_2, X_3, X_4, X_1 and after calculating the window derivatives, the inputs would thus be compared to the expected values: E_2, E_3, E_4, E1.

IV. Test Facilities

A. Texas A&M Heavy Ion Testing

Facility: Texas A&M Cyclotron Facility
Energy: 25MeV/u

Flux: ~10^5 ions/cm^2/s

Fluence: SEU/MBU tests will be run until (1) sufficient statistics are obtained 10^{6} - 10^{7} ions/cm^2 (2) an increase in supply current (I_{dd}) is seen (3) or a SEFI is observed;
SEL tests will be run until (1) an increase in supply current is observed, (2) or a fluence of 10^7 ions/cm^2 is reached.

B. Indiana University Proton Testing

Facility: Indiana University Cyclotron Facility, 75MeV and 200 MeV protons
Flux: 10^6 to 10^7 p/cm^2/s
Fluence: Tests will be run until sufficient statistics are obtained or an increase in supply current (I_{dd}) is seen.

V. Test Conditions and Error Modes (Overview)

Test Temperature: Room Temperature for SEU/SET; up to 85°C for SEL

Tests: Two types of tests were performed. The tests were as follows:

1. Single point: ADC clock and data sinusoid inputs are at the same frequency. Consequently, only one point per sin period is sampled by the ADC and passed to the LCDT.
2. 4 Point: ADC clock is 4x the input data sinusoid frequency. Consequently, the ADC is able to sample 4 points per data period. All four points are passed to the LCDT

Operating Frequency: Clock and Data frequencies are test dependent. ADC clock will range from 10MHz to 100MHz

Power Supply Voltage: V_{dd} = 5V ; I/O = 3.3 V; Stress tests at 5.25V and 4.75V

Data Inputs: Supply Sine Waves from functional generator (as ADC data input) at varying frequencies (test dependent). Supply ADC clock signal at varying frequencies.

Angular Data: Data were taken at 0° (incident angle), 45°, and 60° degrees due to the size constraints of the TI evaluation board.

Recovery from SEL: If SEL is observed, must be able to determine if recovery is possible without power cycling. If recovery does not occur, power supply voltage should be incrementally lowered to determine the point at which recovery is observed. SEL classification will be determined by observing a sharp current jump on the LabView monitor. Current stays at high level.

Monitoring TID: Supply (leakage) current (I_{dd}) was measured after each irradiation to monitor parametric degradation from TID. This was performed for each test.

Data Error Mode:

1) All upsets must be time tagged containing erroneous value and expected value.

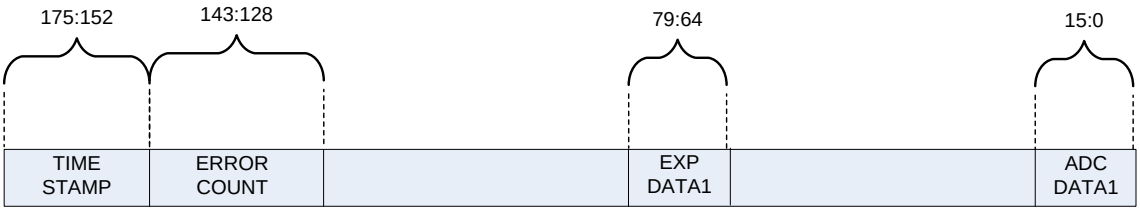


Figure 10: Single Point Data Format. Tester to Host PC Error Word (184 bits total)

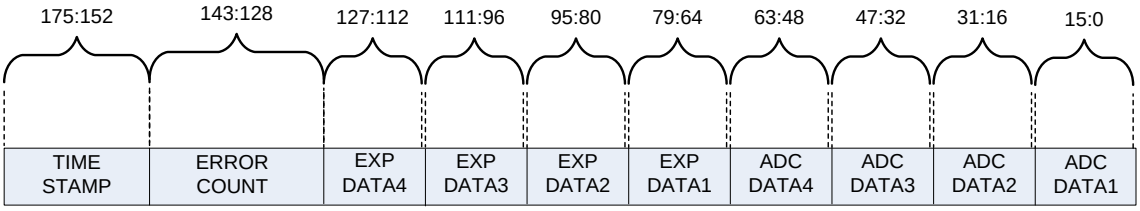


Figure 11:Four Point Data Format. Tester to Host PC Error Word (184 bits total)

2) Error Calculations:

Single point:

- A calculation of the average value ($1x10^6$ samples) will be used as the golden compare.
- Data range settings will be set by user and are utilized in the data comparison

$$val\_low \le Datainput \le val\_high$$

$$val\_low = ExpectedValue - error\_range$$

$$val\_high = ExpectedValue + error\_range$$

- A watchdog is placed on the DRY (ADC data ready signal) to insure that data is streaming at the expected frequency

4 point:

- A calculation of the average value (1024 samples per sample point pre-irradiation) will be used as the golden compare for each of the 4 points

- Data range settings will be set by user and are utilized in the data comparison for all 4 points as in the Single point calculations
- Comparisons to the 4 expected values are performed after 4 points are received from the ADC
- Because of system noise pre-irradiation (generally due to function generators) and SEUs during irradiation, a dynamic 4 point - windowing scheme were implemented in order for the tester to remain synchronous with received ADC data.
- A watchdog is placed on the DRY (ADC data ready signal) to insure that data is streaming at the expected frequency

VI. Running an ADC Test

A. Test Commands

The User controls the tests via a LABVIEW interface running on a PC. The PC communicates with the LCDT with a RS232 serial link. The format of communication is a command/Data 4 byte word.

Table 1 : Summary of Commands Used in Eclipse Tester

Command #HEX	Command	D0	D1	D2	Description
01	Reset DUT	N	N	N	Resets Tester
02	Start Test	N	N	N	Starts gathering ADC data
B0	Error Range	Y	N	N	(exp value-Error_range) < ADCout < (exp value+Error_range);[0 … 255]; default=0
90	Test Number	Y	N	N	Selects ration of clock to data {0..2}
A0	Clock Frequency	Y	N	N	Clock frequency divider of 100mhz; [2...255] default = 1

The following is a detailed description of commands and their associated functionality.

1. RESET DUT:

The RESET DUT command is decoded as x01. The following represents the command as noted in Table 1:

x01	xx	xx	xx

Figure 12: Reset Command Format – Command Number, D0, D1, and D2

Once decoded, all DUT inputs will go into reset mode (Reset, CLK_SR and D_SR are low)

2. START TEST:

START TEST is decoded as x02. The following represents the command as noted in Table 1:

x02	xx	xx	xx

Figure 13: Start Command Format

All other commands should be supplied before start test. I.e. the user should define the pattern and clock frequency before administering a start. This command activates the CLK_SR and D_SR DUT inputs.

3. Error Rage:

Error Range is decoded as xB0. The following represents the command as noted in Table 1:

xB0	xnn	xx	xx

Figure 14: Start Command Format

This command must be supplied before the start test (unless using the default value= 0).

4. Test Number:

Test Number is decoded as x90. The following represents the command as noted in Table 1:

x90	xnn	xx	xx

Figure 15: Start Command Format

This command must be supplied before the start test (unless using the default value= 0).

Xnn = 0: SINGLE POINT TEST (samples are 1 per sin wave period)

Xnn = 1: 4 POINT TEST (samples are 4 per sin wave period)

5. CLOCK FREQUECY:

The clock frequency command is decoded as xA0 utilizing byte D0. The following represents the command as noted in Figure 16:

xA0	xnn	xx	xx

Figure 16: Clock Frequency Command Format

Upon the receipt of this command, D0 is used as a clock frequency divider. This command must be sent after a RESET DUT and before a START TEST. D0 must be an even number and must be greater than or equal to 2. The associated output is CLOCK_FREQ. See the LCDT General Tester for more information concerning the processing of CLOCK_FREQ.

B. Specific Steps towards Running an ADC Test

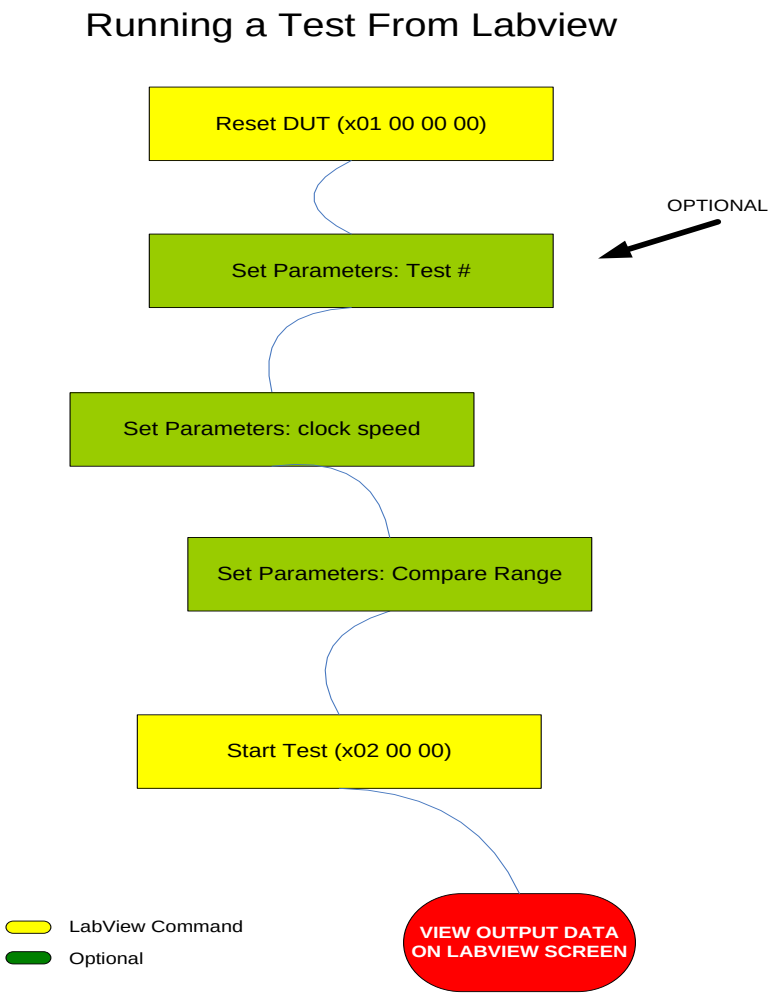


Figure 17: Flow Diagram of Running an ADS5483 Radiation Test

VII. Test Results

A. Texas A&M Cyclotron Heavy Ion Radiation Tests

The ADS5483 DUT was tested at the Texas A&M University Cyclotron Single Event Effects Test Facility using a 15MeV/u Tune at room temperature. All tests were run with 10^3<flux rate < 10^4. Effective LETs ranged from 2.5MeV*cm^2/mg to 83.4 MeV*cm^2/mg by varying the ion and by varying the angle of incidence.

Ion	Initial Energy (MeV)	Angle	Initial LET (MeV•cm^2/mg)
Ne	250	0°	2.5
Ne	250	45°	3.5
Ne	250	60°	5
Ar	496	0°	9.6
Ar	496	45°	13.6
Ar	496	60°	19.2
Cu	560	0°	22.7
Cu	560	45°	32.1
Cu	560	60°	45.4
Ag	720	0°	49.2
Ag	720	45°	69.5
Xe	940	0°	53.9
Xe	940	45°	83.4

Regarding the following sections, cross sections are generally calculated by:

$$\frac{\#\,Events}{fluence(\#\,ion\ particles)}$$

There will be error cross sections that reflect total events and others that reflect a specific type of event (e.g. a burst).

B. Heavy Ion Results and Analysis for FP Test Data

Error signatures and their severity are important information that must be provided to design teams of critical systems. As previously stated, if a signal flattens or significant phase shifts occur, the tests should be able to detect the events, their longevity, and be

able to differentiate such events. It will be proven that the FP test methodology facilitates these requirements.

All graphs in this section that reflect ADC output codes versus time were constructed from FP SEU radiation tests. As described in the previous section, expected ADC output values were automatically calculated prior to each radiation test run by the LCDT. Graphs that contain data points reflect erroneous ADC output codes accompanied by their expected code values. The graphs are EXCEL spreadsheet point-to-point fits.

1. Cross Section Evaluation

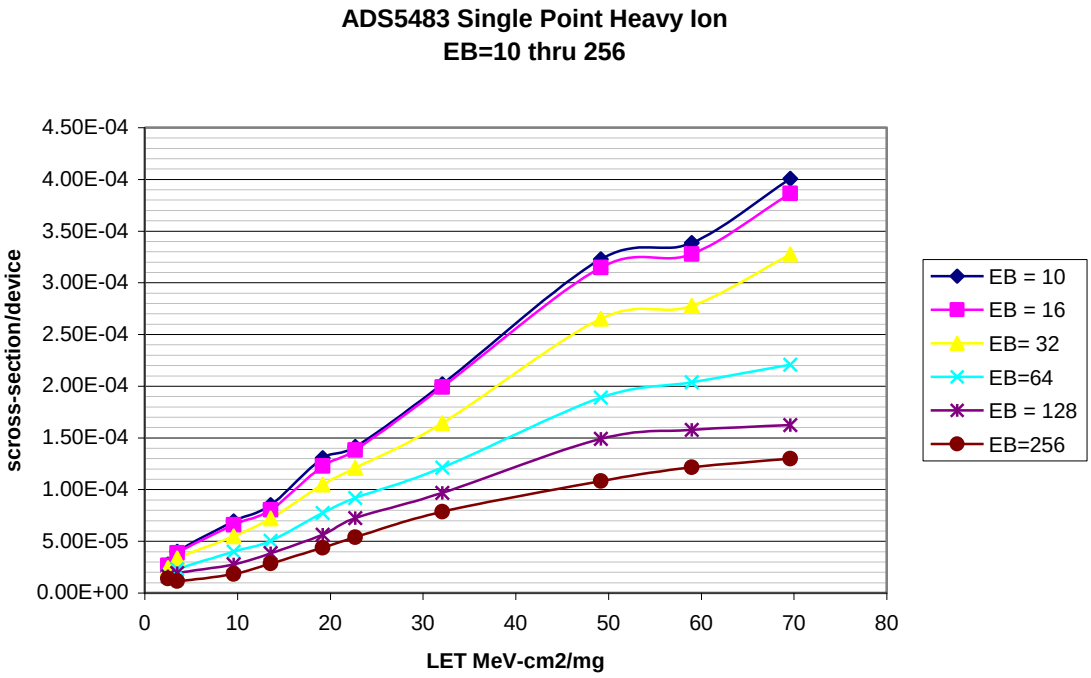


Figure 18: TIADS5483 Single Point Heavy Ion Error Cross Sections with varying Error Bounds (EB)

Figure 18 illustrates the error cross sections versus LET for a variety of EBs. At the lower LETs, EB does not significantly affect the error cross section. This is because most of the code errors have large amplitude differences (from the expected value) and are not filtered by the EBs. At the higher LETs, the code errors are a mixture large and small amplitude offsets.

2. Burst Evaluation

A differentiation has been made between errors that are only one cycle in duration (see Figure 19) vs. multiple cycles. For this manuscript, a burst is defined as the DUT being upset for multiple cycles do to a particle hit. Further evaluation of the types of upsets

was performed including burst frequency vs. single cycle frequency per LET with various EBs.

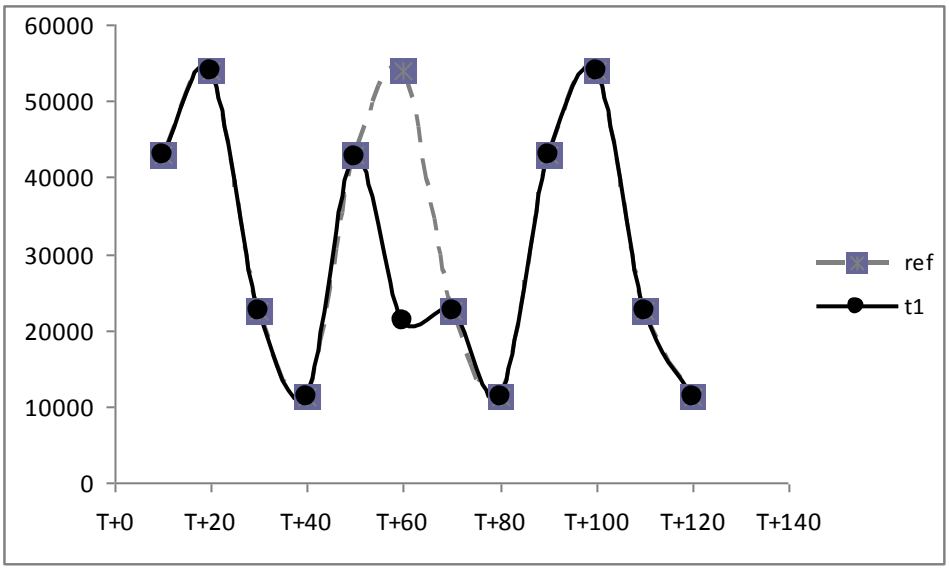


Figure 19: Single Cycle Upset During a Heavy Ion Radiation Test. Dashed curve is the actual pre-calcualted expected values prior to the test. The solid curve contains the ADC outputs during radiation exposure. This is an example of only one point deviating from its expected value. Expected and SEU data points are gathered from run#63 within the heavy ion suite of tests

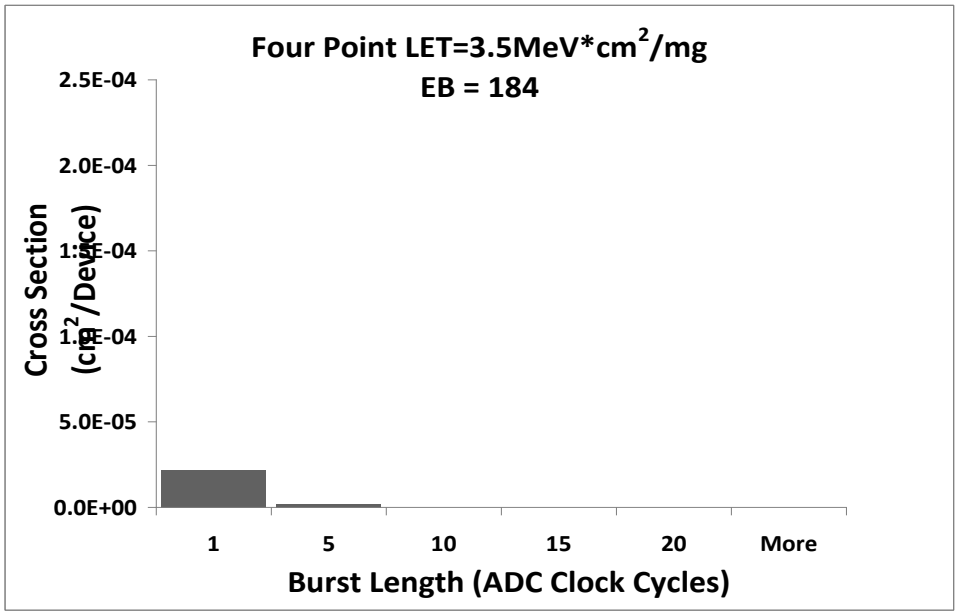


Figure 20: Burst Length versus Error Cross section (Burst Frequency/Particles/cm^2) f or LET=3.5MeVcm2/mg and the lowest EB utilized for the FP testing (184=2.8mV mask)

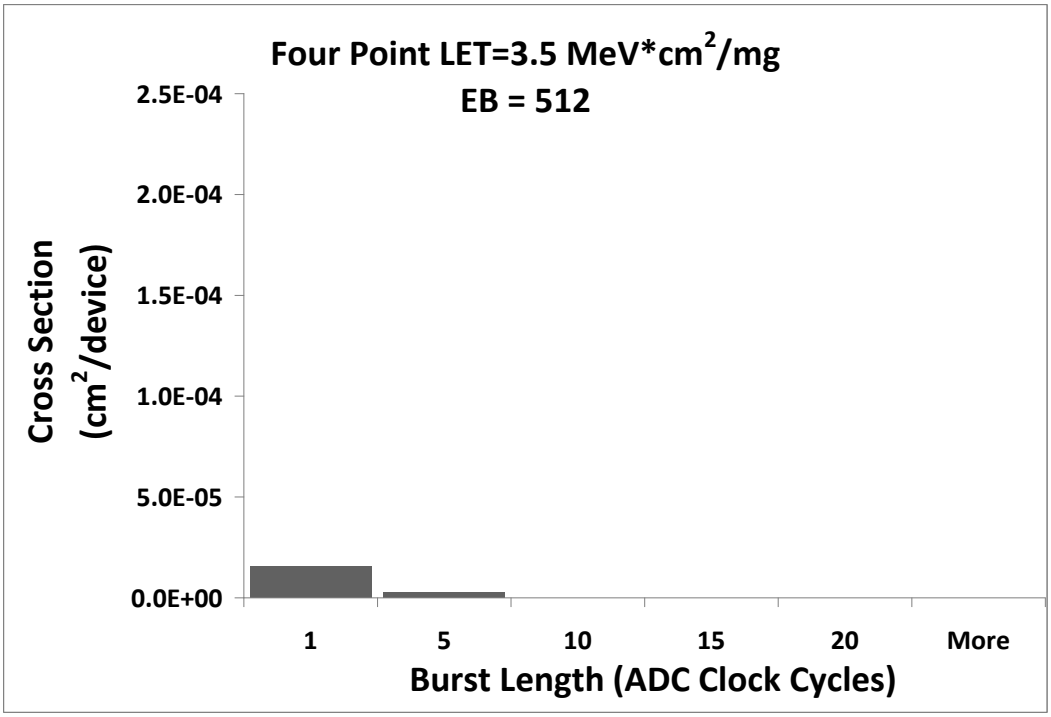


Figure 21: Burst Length versus Error Cross section (Burst Frequency/Particles/cm^2) f or LET=3.5MeVcm2/mg and the lowest EB utilized for the FP testing (512=7.8mV mask)

Regarding Figure 20 and Figure 21, there is not a significant difference between the upsets at 3.5MeVcm^2/mg EB=184 and EB=512. This is as expected and is also illustrated in the SP Error cross section graph (Figure 18). Figure 20 and Figure 21 suggest that at low LETs, most of the errors are single cycle upsets with large amplitude offsets from the expected value.

Figure 22 and Figure 23 illustrate that at higher LETs (32.1 MeVcm^2/mg), the cross sections are approximately 50% lower at an EB=512 vs. EB=184. The number of bursts is becoming more significant at the higher LETs. It is the bursts that contain a larger percentage of upsets with small amplitude upsets. This is because most of the small amplitude upsets have a signature of jittering around their expected values (small perturbations due to analog circuitry upsets).

At LETs greater than 59 MeVcm^2/mg, bursts have been observed with durations 39 cycles, 69.9 180 cycles, 83.4 39 cycles.

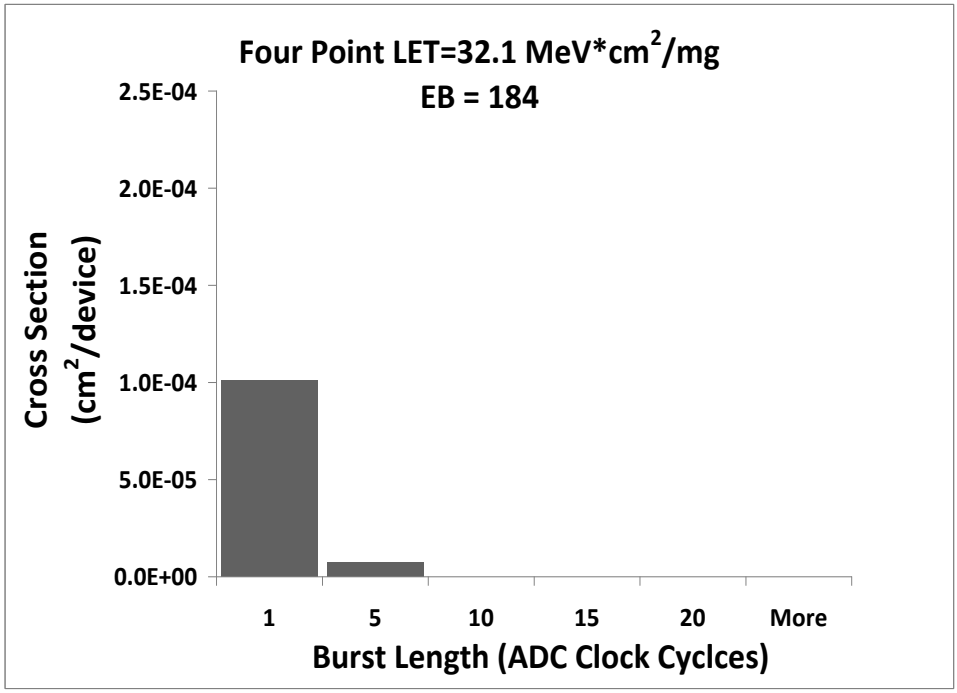


Figure 22: Burst Length versus Error Cross section (Burst Frequency/Particles/cm^2) f or LET=32.1MeVcm^2/mg and the lowest EB utilized for the FP testing (184=2.8mV mask)

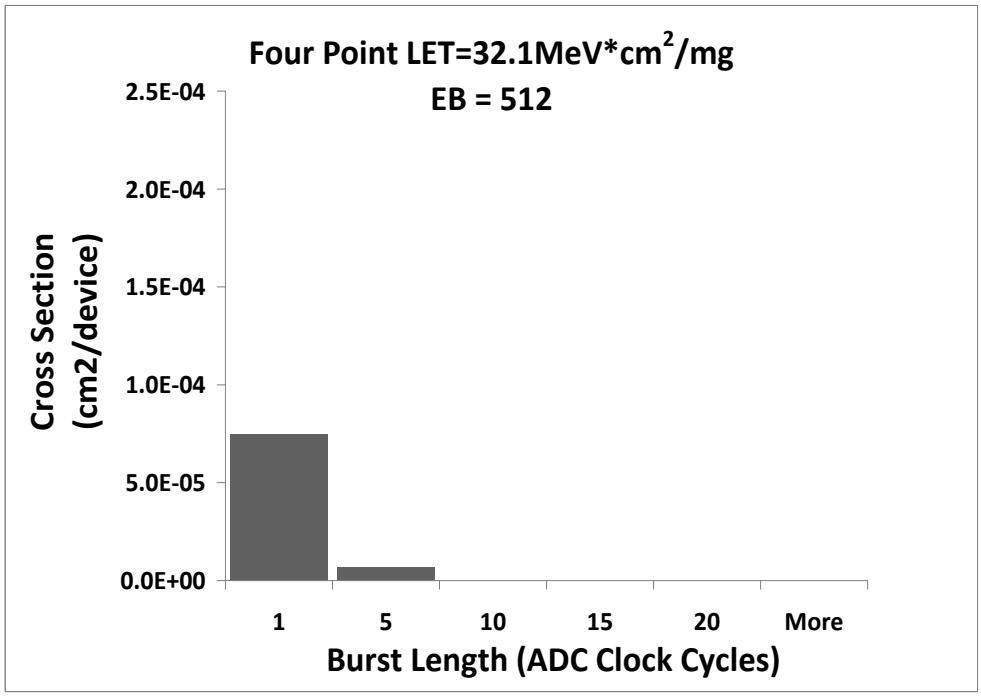


Figure 23: Burst Length versus Error Cross section (Burst Frequency/Particles/cm^2) f or LET=32.1MeVcm^2/mg and the lowest EB utilized for the FP testing (184=2.8mV mask)

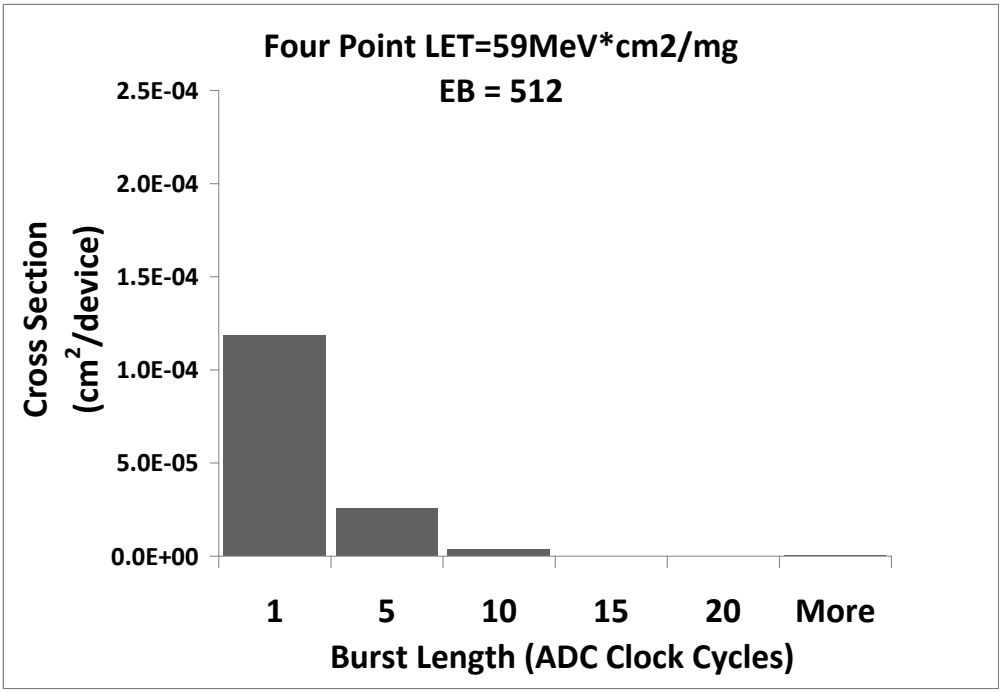


Figure 24: Burst Length versus Error Cross section (Burst Frequency/Particles/cm^2) for LET=59 MeVcm^2/mg and the lowest EB utilized for the FP testing (184=2.8mV mask)

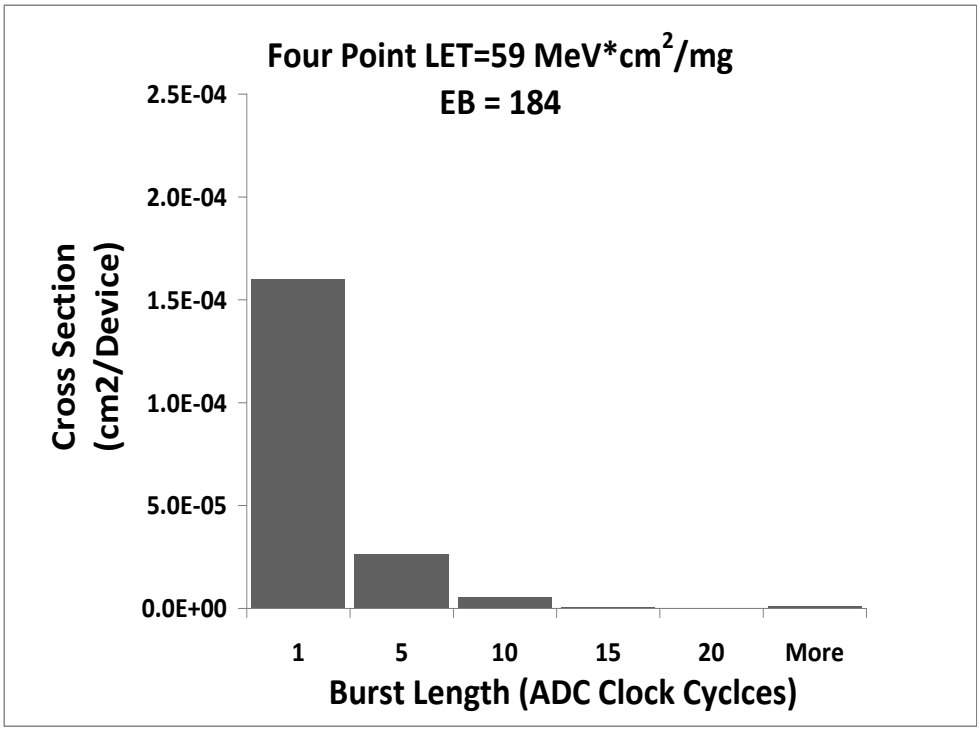


Figure 25: Burst Length versus Error Cross section (Burst Frequency/Particles/cm^2) for LET=59 MeVcm^2/mg and the lowest EB utilized for the FP testing (512 =7.8mV mask)

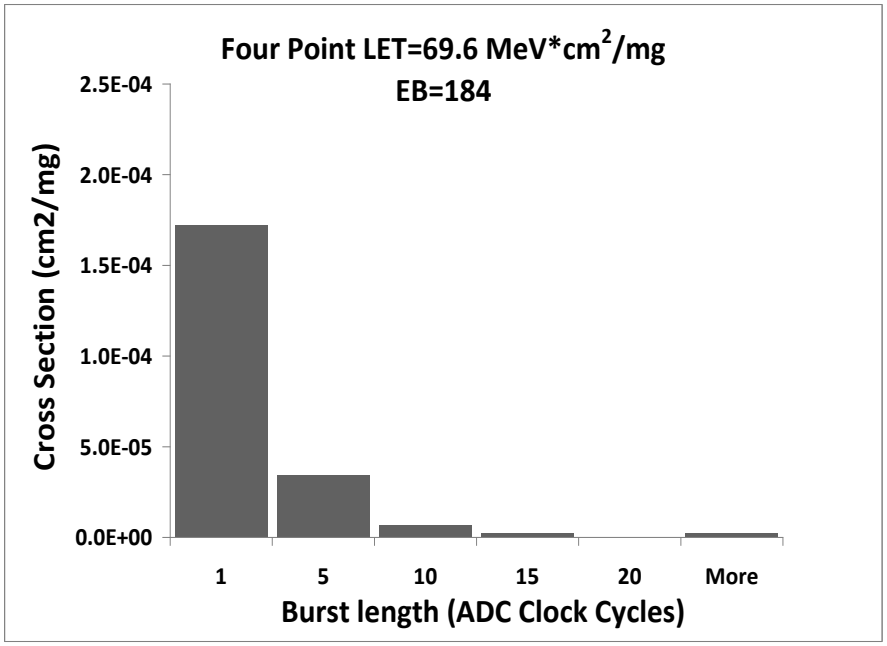


Figure 26 Burst Length versus Error Cross section (Burst Frequency/Particles/cm^2) for LET=69.9 MeVcm^2/mg and the lowest EB utilized for the FP testing (184=2.8mV mask)

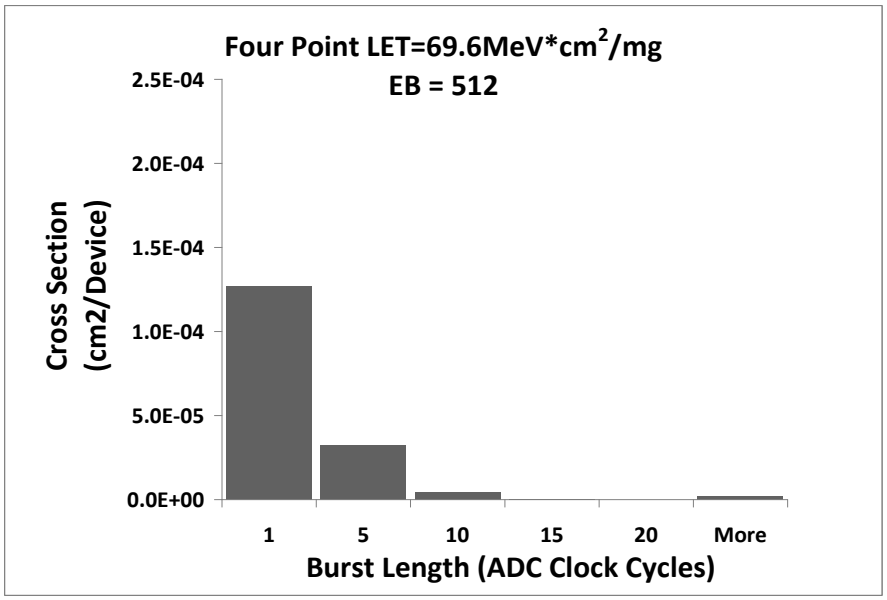


Figure 27 Burst Length versus Error Cross section (Burst Frequency/Particles/cm^2) for LET=69.9 MeVcm^2/mg and the lowest EB utilized for the FP testing (512=7.8mV mask)

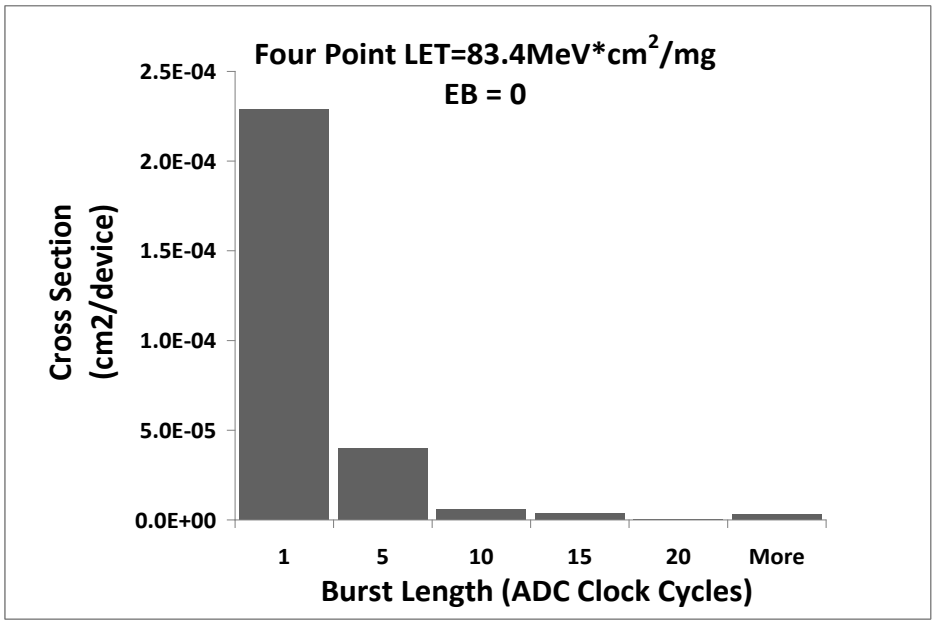


Figure 28: Burst Length versus Error Cross section (Burst Frequency/Particles/cm^2) for LET=83.4. MeVcm^2/mg and the lowest EB utilized for the FP testing (184=2.8mV mask)

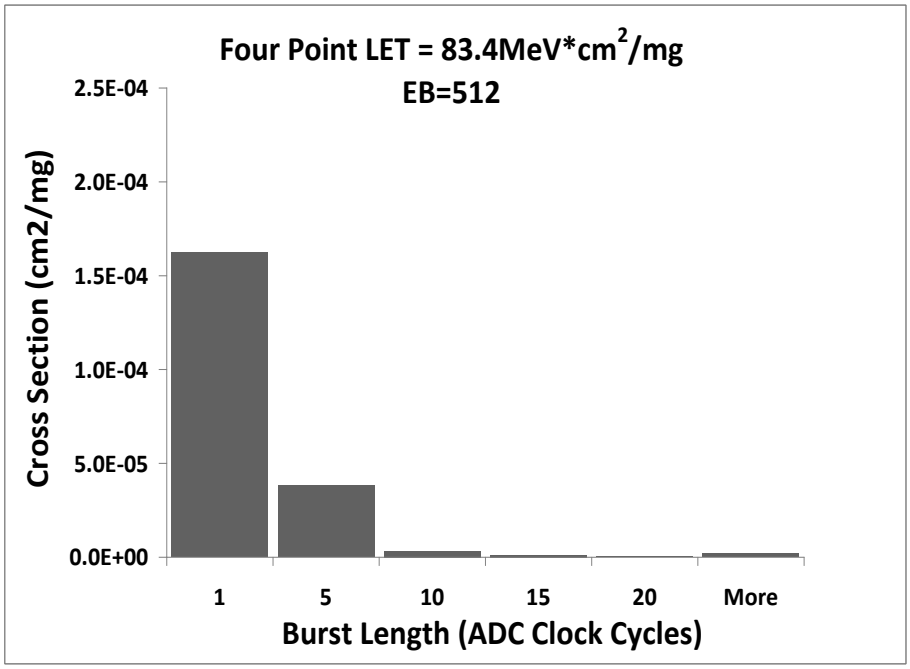


Figure 29: Burst Length versus Error Cross section (Burst Frequency/Particles/cm^2) for LET=83.4 MeVcm^2/mg and the lowest EB utilized for the FP testing (512=7.8mV mask)

3. Signal Composition and Distortion Evaluation

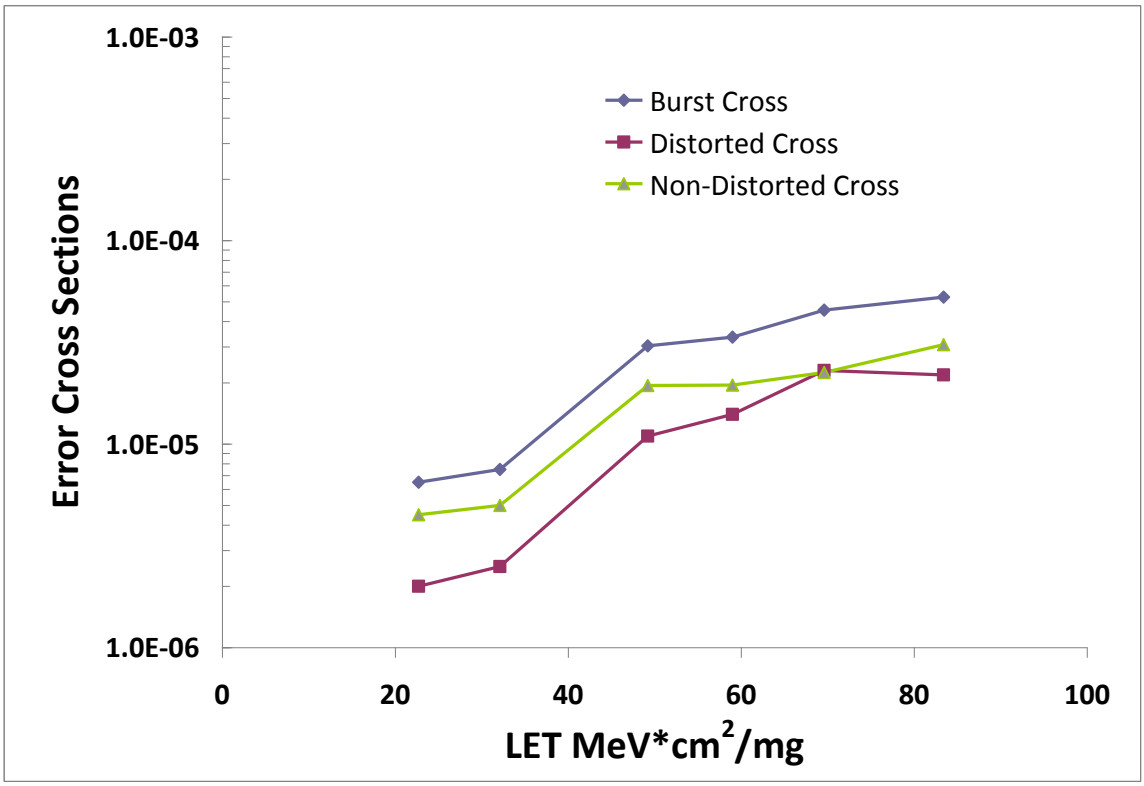


Figure 30: Heavy Ion Distorted vs. non-distorted Bursts. Data does not include upsets that are single-cycle duration (i.e. only burst cross sections are compared)

Figure 30 is a comparison of non-distorted bursts to distorted bursts. It is important to note that the error cross sections graphed in this figure do not include upsets that have single cycle duration. Only bursts are considered in Figure 30. This evaluation was performed to identify bursts of upsets that maintain their signal composition versus bursts that do not. In most cases, a burst that does maintain composition is a phase shift of the output. A burst that does not maintain its composition is a more complex upset (such as signal flattening, clock loss, temporary stuck bits, etc…). At the lower LETs, most of the bursts keep their composition. However, as the LETs increases, the percentage of bursts that are distorted because significantly equivalent to the non-distorted bursts.

C. Indiana University Proton Radiation Tests

Data was obtained for two energies at the Indiana University Cyclotron: 78Mev and 198MeV. Error Cross sections were calculated as:

$$\frac{\#\,Events}{\#\,fluence(\#\,protons)}$$

1. Cross Section Evaluation

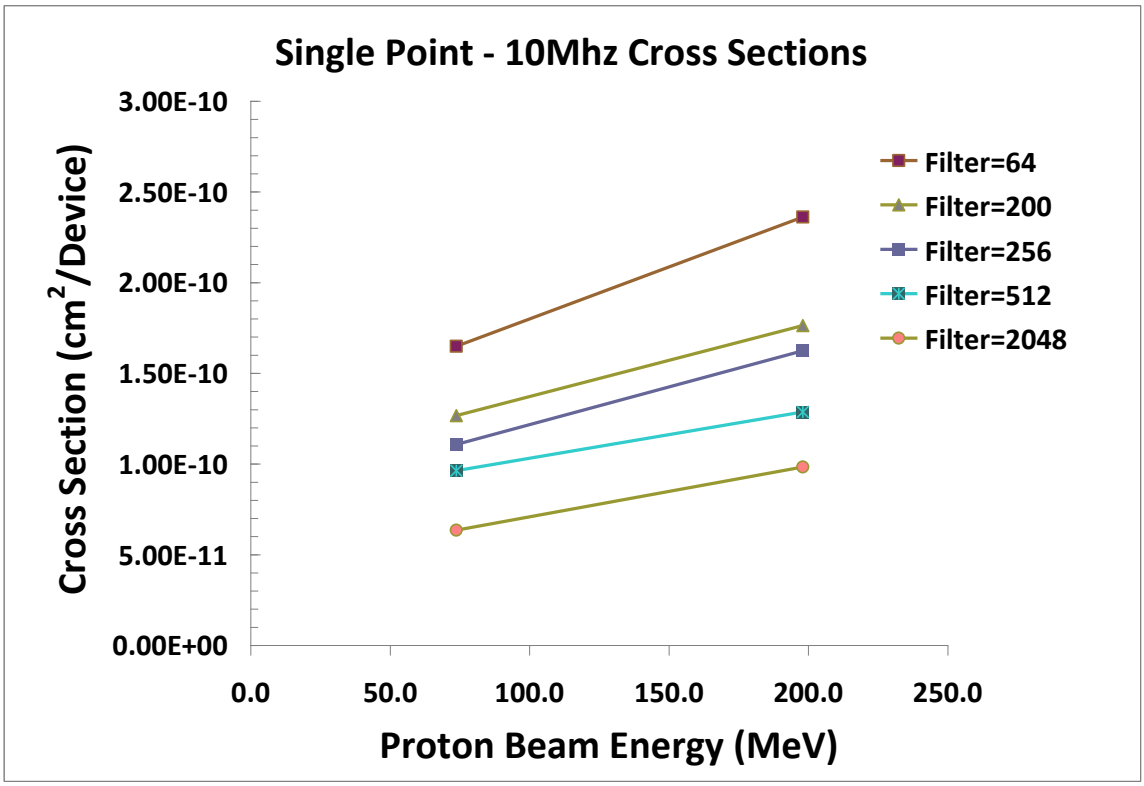


Figure 31: Single Point Error Cross Sections for ADC Clock and Data at 10MHz. (Filter stands for EB in this figure)

Figure 31 and Figure 32 show the error cross sections per proton energy at 10MHz and 100MHz SP test modes (ADC Clock frequency = ADC Data frequency). The difference in cross sections is statistically insignificant between the two frequencies. This suggests that ADS5483 SEU cross sections due to protons are not frequency dependent.

As the EB (filter) is increased, the cross sections decrease as expected for both energies tested (73.7MeV and 198MeV). However, the slope of the segment connecting 73.7MeV to 198MeV increases at the lower EBs. This shows that at higher energies there is a percentage increase in the number of smaller offset errors than that of the larger amplitude errors. As matter of fact, many errors at the higher energies are long bursts that jitter around the expected values (upsets with small amplitudes). This is evident in the following section discussing bursts.

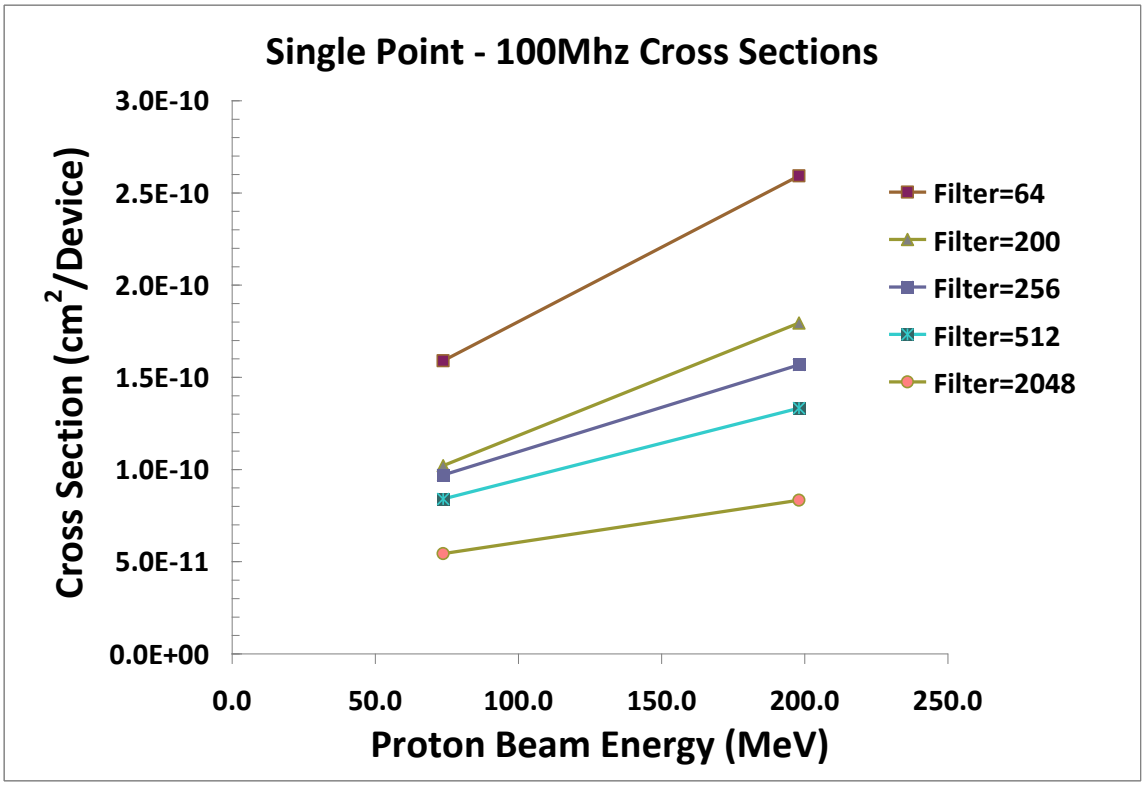


Figure 32: Single Point Error Cross Section for ADC clock and data = 100MHz. Error Cross Sections for SP=10MHz and SP=100MHz are statistically equivalent. Proves Clock frequency has little to no affect on SEE sensitivity (Filter stands for EB in this figure)

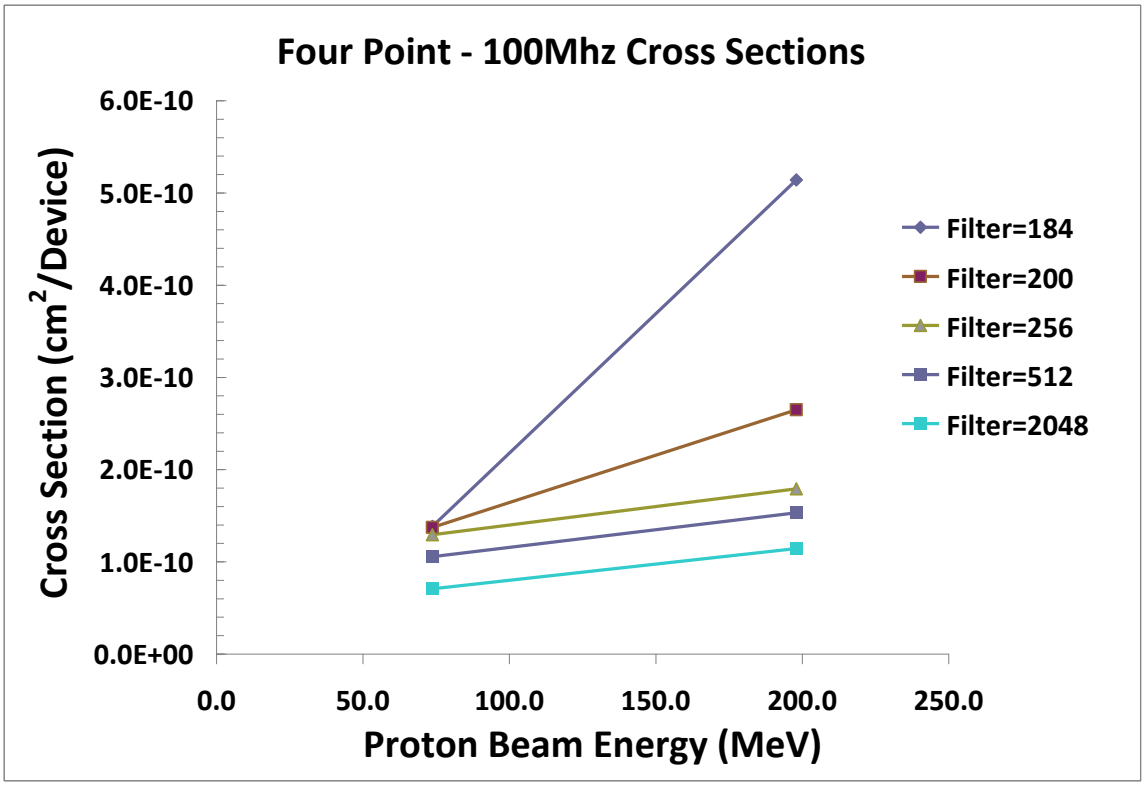


Figure 33: Observed more upsets than the single point below 512 EB. The FP method seemed to be a bit more sensitive to observing some errors than the SP method. This is under investigation.

The four point error cross sections show a much larger cross section at 198MeV than the single. As the filters increase, the SP and FP cross sections agree. The FP was able to detect more of the jitter upsets than the SP method. The reason is currently under investigation. However, as in the SP cross sections, one can see that the higher energies have a larger percentage of small errors than the lower energies (slope of EB curves).

2. Burst Evaluation

It is very interesting that the proton tests produced upsets with much longer bursts than heavy ions. The longest burst observed under heavy ion tests was 39 ADC cycles. The longest bursts observed with protons (at 198MeV and EB=184) lasted for 1000's of ADC clock cycles. The long bursts only consist of jitter points and are very small perturbations from the expected value. The difference between the burst lengths observed with an EB=184 vs EB=512 are significant. Burst lengths are lower than 2000 (EB= 512) cycles versus 5000 (EB= 184). Also, at EB= 512 one can see that the percentage of single cycle errors has significantly increased versus EB=184.

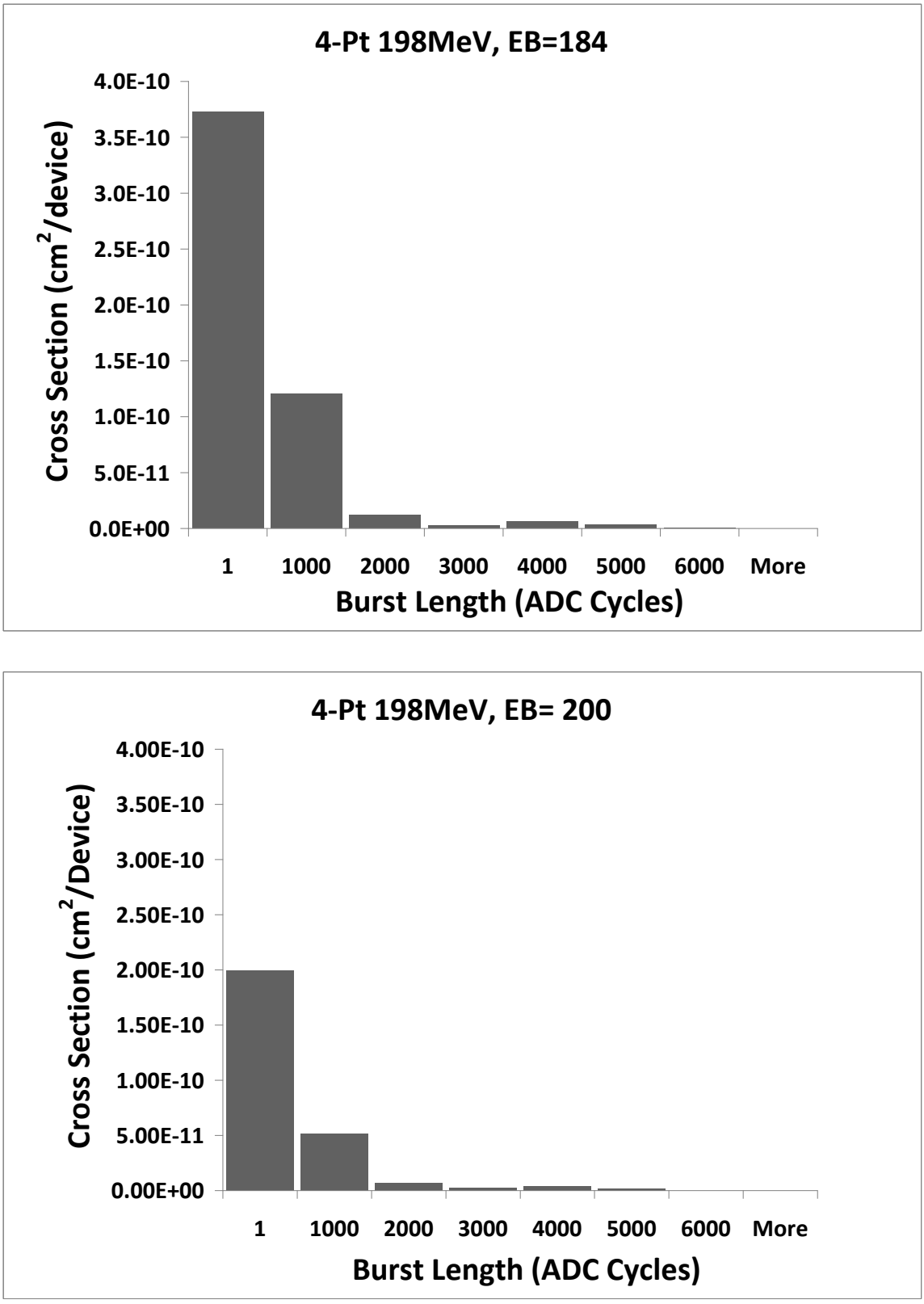


Figure 34: Significant decrease in FP Burst cross sections. However, burst length ratios remain the same

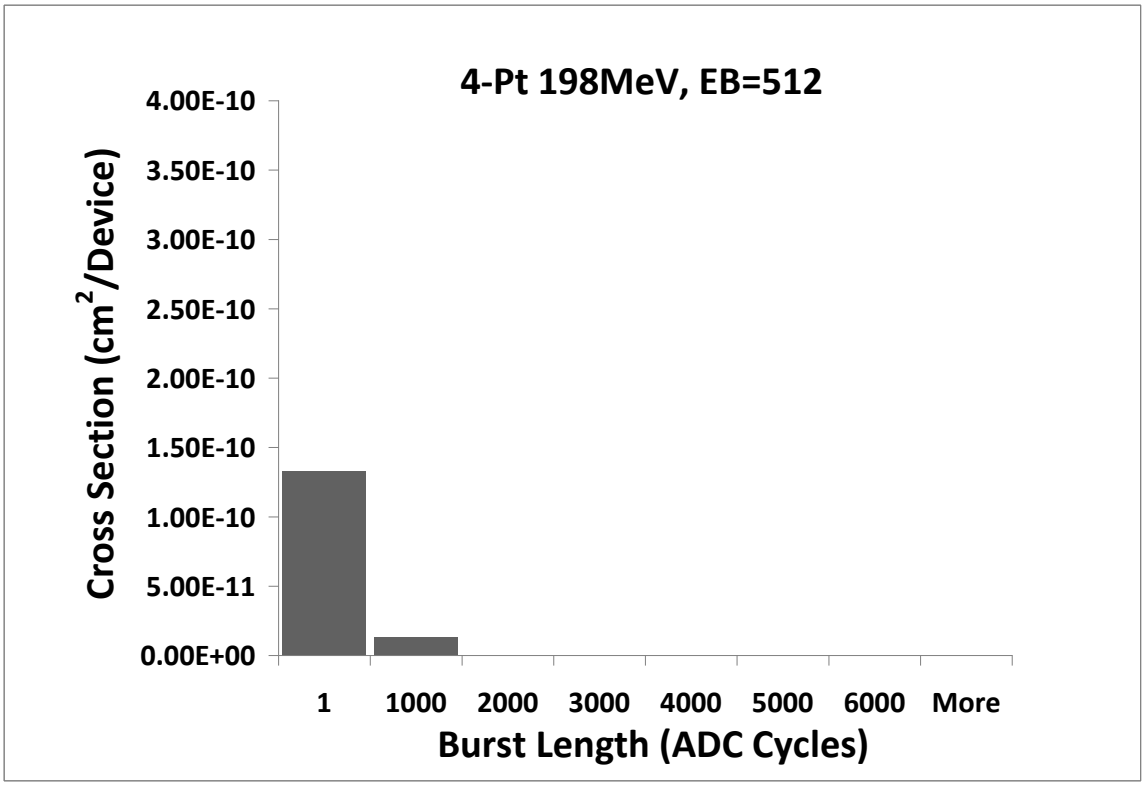


Figure 35: long Bursts disappear with an EB=512 (7.8mV) – most long bursts at lower EBs were all within 7.8mV from expected values. The bursts were jittering around expected values suggesting analog clock circuitry, analog reference, or regulator upsets.

At the lower energy of 73.4, the number of bursts and their lengths were insignificant as illustrated in Figure 36.

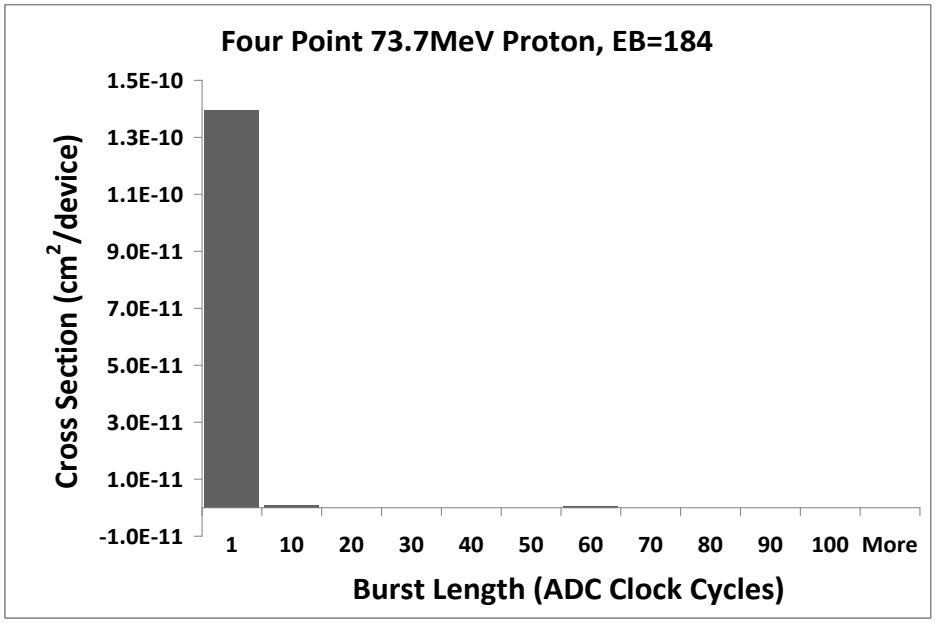


Figure 36: 73.7 MeV protons do not cause long bursts as with the 198MeV protons. Most upsets are single point with very few bursts.

3. Signal Composition and Distortion Evaluation

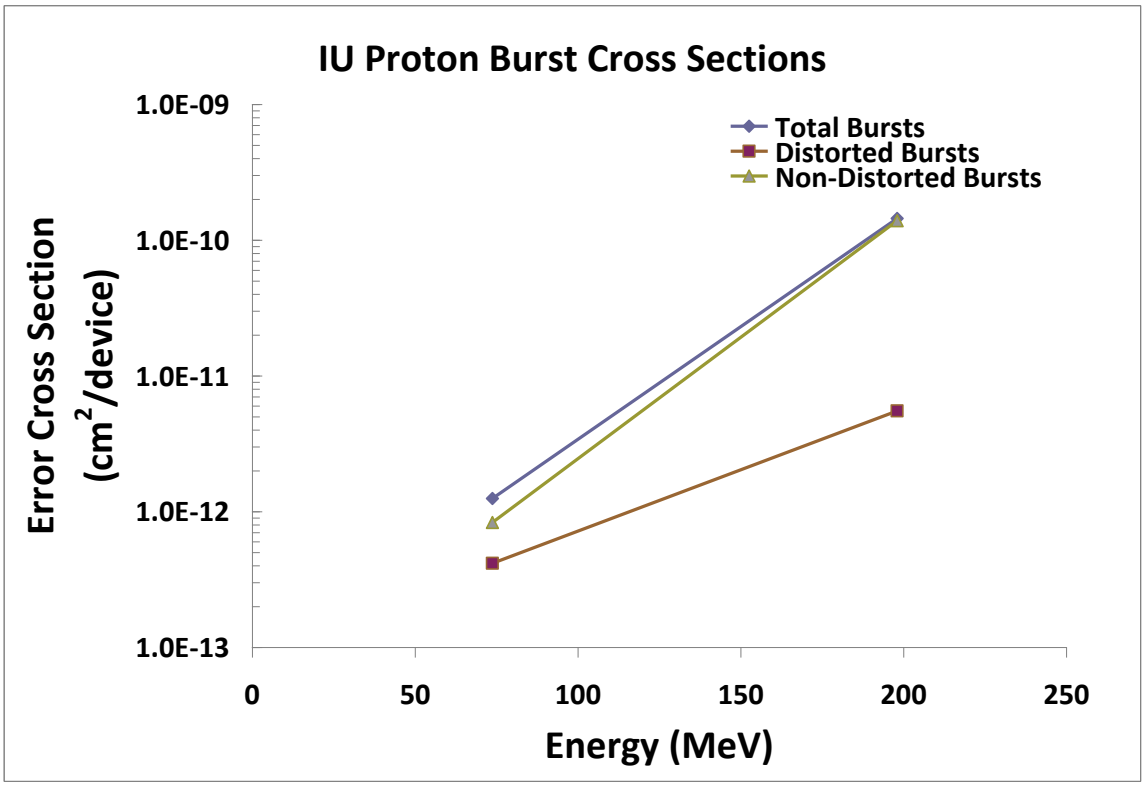


Figure 37: All Burst Cross Sections were measured with FP Method

Figure 37 illustrates that at the higher energies, most of the bursts are non-distorted – this suggests jitter or phase shift and corresponds to what we observed in the previous analysis.

VIII. Summary

1. The SEU/SET response of the ADS5483 consists of:
    a. Code upsets that only last for one ADC clock cycle
    b. Code upsets that last for multiple ADC clock cycles (bursts)
        i. Heavy Ion bursts were not as frequent as proton bursts. The longest Heavy ion burst lasted for 39 cycles
        ii. Bursts due to 198 MeV Proton strikes could last thousands of cycles. However, at 7.8mV and above, the burst duration and frequency is significantly reduced. This is due to the fact that most of the burst upsets were small upsets from the expected values – i.e. the errors jittered around the expected values. This suggests that the analog circuitry has a significant sensitivity to protons with 198MeV energy.
        iii. Most upsets due to 73 MeV protons were single cycle upsets.
2. No clock losses were observed – however, this is still under investigation
3. SEU/SET rate did not increase significantly with frequency (10MHz vs. 100MHz)

If the user is planning on using this device in a proton rich environment, attention must

be given to the granularity of error range. An error range of 10mV will reduce the impact of prolonged burst upsets and enable better accuracy during averaging and frequency domain analysis of the ADC input signal.